National Action Plan for U.S. Leadership in Advanced Compute & Microelectronics

Context: Why Now

We are entering an era where exponential gains in compute and microelectronics are no longer assured. Disruptive technologies are emerging that could change the nature of compute, and U.S. leadership cannot be left to chance.

Desired Endstate: The Future

The United States dominates the post-Moore's Law future by bringing the world into the era of heterogeneous integration, scaling breakthroughs across the compute stack, and establishing positions of advantage in new forms of computing.

Central Policy: How to Achieve

Chart a post-Moore's Law future by catalyzing disruptive innovation via compute moonshots and building a flourishing atoms-to-architectures innovation pipeline that can develop, scale, and integrate novel materials and devices.

Action Plan Overview

1	**1: Launch: Scale Emerging Compute Paradigms via National Moonshot Programs** 1.1: Integrate Multiple Forms of Advanced Compute via Hybrid Computing 1.2: Create a One Million Qubit Fault-Tolerant Quantum Computer by 2028 1.3: Improve Compute Energy Efficiency by 1,000x to 1,000,000x 1.4: Lead in Scaling Superconducting Electronics
2	**2: Organize: Closing Gaps in the Microelectronics Innovation Ecosystem** 2.1: Organize the NSTC to Pursue DARPA-like Programs 2.2: Optimize the NSTC Investment Fund to Pursue Disruptive Innovation 2.3: Augment the NSTC with an Incubator Function
3	**3: Research: Fund and Attract Microelectronics R&D** 3.1: Fuel Public Microelectronics R&D for Long-Term Competition 3.2: Crowd-In Industry R&D Funding Through Tax Policy
4	**4: Scale: Enabling Technologies for Future Compute & Microelectronics** 4.1: Unleash AI-Powered Chip Design Tools 4.2: Build Digital Twins for Compute & Microelectronics R&D 4.3: Scale the Materials Genome Initiative for AI-Enabled Materials Discovery 4.4: Reshape Microelectronics Fabrication via Fab-in-a-Box Approaches 4.5: Pursue Technological Leadership in Advanced Packaging & Chiplets 4.6: Unleash Next-Generation Lithography by Deepening Public-Private Partnerships 4.7: Offer Cryogenic Refrigeration as a Service
5	**5: Assure: International Collaboration for Secure Microelectronics** 5.1: Boost R&D Collaboration on Secure Microelectronics with Trusted Partners 5.2: Increase International Collaboration on Legacy Chips 5.3: Develop Labeling and Certification Requirements for Microelectronics Used in U.S. and Allied Critical Infrastructure Sectors 5.4: Promote Robust Critical Infrastructure Security Standards with Allies and Partners
6	**6: People: Cultivate, Attract, and Retain Microelectronics Talent** 6.1: Attract International Microelectronics Talent 6.2: Nurture Communities of Engineering Practice in Emerging Paradigms 6.3: Scale the "Custom Silicon" Effort for College Student Experiments